

California Institute of Technology  
Department of Computer Science  
Computer Architecture

CS184b, Winter 2000

Assignment 8: VM

Thursday, February 22

**Due:** Thursday, March 1, 5:00PM

**Part A** Work the following problems from Hennessey and Patterson:

- 5.8
- 5.19
- 5.20

**Part B**

1. Make a rough estimate of the cycles lost servicing a TLB miss.
  - Aside from TLB, use default memory system times from simplescalar.
  - Think about pipeline flush/restart.
  - Think about minimum state storage/recovery on each side of the context switch.
  - Sketch actions in “kernel” to update the TLB (doesn’t need to be runnable assembly, but should be enough that you can estimate an instruction and cycle count from).
  - Think about caching/cache-pollution effects.
  - State additional assumptions you make about the machine in order to develop and ground your answer.

I’m mostly interested in having you take the time to think through all the actions and think about the relative impact of the various components.

2. I believe your applications are moderately small. Use simplescalar tools to answer.
  - How small can the TLBs be to just fit your application (minimum size so no capacity misses, minimum associativity to avoid conflict misses for itlb and dtlb)?
  - Assuming an itlb miss latency as estimated in the previous question, how much smaller can you make the TLB without having a significant impact on performance?