

California Institute of Technology  
Department of Computer Science  
Computer Architecture

CS184b, Winter 2000

Assignment 5: ILP

Tuesday, January 30

**Due:** Tuesday, February 6, 5:00PM

1. Work HP 4.10
2. Use `sim-outorder` on your chosen program to compare 4 cases
  - simple-pipe case (from last two assignments)
  - default `sim-outorder` machine
  - default `sim-outorder` machine, except `inorder` issue
  - “ideal” case (which you create by setting various parameters to large values so will be non-limiting)
3. Using default sizes (and default machine configuration), compare the performance of the three branch history options given (bimodal, 2-level, combining). How well does branch prediction accuracy correlate with performance?
4. Balance the resources in the `sim-outorder` pipeline, starting from the default `sim-outorder` machine. Keep fetch queue at 4, and try to make everything else in the pipeline just large enough to not be the limiting factor on performance, but not larger. (maybe target a goal of performance within 10% only fetch is at 4 and everything else is “ideal”). You probably want to do a sensitivity analysis for each resource to determine what’s limiting and how to change.
5. A first-order model for the area of branch prediction and target support is to count memory bits.
  - For `sim-outorder`’s default scheme (bimodal), how many total memory bits are used to optimize branching? (bimodal = simple 2b counter scheme discussed in class and in text; include branch table, return address stack)
  - Sticking with the bimodal prediction scheme only, assuming you have twice as many bits as you calculated above, what is the best way to (re)allocate those bits? (use the simulator to explore different prediction schemes and allocations)