California Institute of Technology
Department of Computer Science
Computer Architecture

CS184b, Spring 2003 Assignment 6: Comm. Impact Monday, May 12

Due: plan – Friday, May 16, 5:00PM
Due: report – Friday , May 30, 11:59PM

Develop a fine-grained, parallel streaming compression application and metric the impact of communication overhead/latency on application performance and exploitable parallelism.

- Develop fine-grained parallel streaming implementation for compression application – this should probably be parameterized so you can tune the parallelism (number of threads) used by the application.
- Add streaming operations (strmrd, strmwr) to SimpleScalar with options to control cycles required on processor and latency for communication; you will need to be able to connect streams between different SimpleScalar processes; you need to think about cycle synchronization between communicating SimpleScalar processes.
- Provide system support to link together SimpleScalar simulation processes running on the same machine and on multiple machines.
- For various levels of parallelism report on speedup obtainable as a function of the strmrd/strmwr parameters; identify the points in these curves which model the mechanisms you measured in assignment #5.
- Time the simulation itself while performing the above experiments. Report on the speedup for the multi-process SimpleScalar simulation for various machine/processor configurations.

Please continue to work as a group for this assignment. Divide work. Support each other in developing experiments, analysis, collecting and corroborating results.

You may want to look at:

- Technical Report `/cs/courses/cs184/software/simplescalar/TR_1342.ps`
- Slides on using (and modifying) SimpleScalar `/cs/courses/cs184/software/simplescalar/simplesim-3.0/hack_guide.pdf`
- Other documentation on `www.simplescalar.com`

Possible Division of development labor:

- Develop application (1)
- Modify SimpleScalar (2) – nominally, maybe one person specializing on adding instruction, second on providing communications to/from SimpleScalar process.
- Link Together SimpleScalar simulations (2?)

Turnin:

Plan: Who's doing what; 1–2 paragraph per person, including brief sketch of how will attack your subproblem.

Report:

1. Documented application source and text description of decomposition and parallelism parameters, including design rationale.
2. Documented excerpts of changes to SimpleScalar with text dscribing the changes and how the streaming operations work.
3. Documented source for simulation assembly with text description.
4. Please indicate clearly who wrote which of the above sections.
5. Results of streaming parameter exploration with text discussion of results and conclusions. Summarize the relationships among parallelism, processor cycles per strmrd/strmwr, and process-to-process latency in a few graphs.
6. Results on parallelism and speedup for simulation and text discussion of results and conclusions.